REMARKS

Claims 1-13, 15-21, and 23-27 will be pending in the current Application. Claims 5, 10, 13, 15, 18, 21, 24, and 25 have been amended; claims 14 and 22 have been cancelled; and claims 26-27 have been added. Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Specification

The Examiner has indicated that the title "Processing System Having Sequential Address Indicator Signals" is not descriptive. However, Applicants respectfully disagree. Each of the independent claims relate to a processing system which has one or more sequence signals to indicate information about the sequentiality of addresses. Therefore, Applicants respectfully submit that the title is descriptive, and no amendment to the title is necessary.

Claim Objections

Applicants have amended each of claims 5, 13, and 18 to replace "decode unit" with – decode control unit – as requested by the Examiner.

Claim Rejections under 35 U.S.C. § 102

Claims 1-9, 13-17, and 21-25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,604,877 to Hoyt et al. (hereinafter "Hoyt"). Claims 10-12 and 18-20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,205,536 to Toyohiko Yoshida (hereinafter "Yoshida"). Applicants respectfully traverse the rejections.

Claims 1 and 3 and their Dependent Claims

Claims 1 and 3 each include generating a first sequence signal that when negated indicates that the current address may not be sequential to the previous address, a second sequence signal that when negated indicates that the current address is not sequential to the previous address, and a third sequence signal that when negated indicates that the current address, if it is an instruction address, is not sequential to an immediately preceding instruction address and when asserted indicates that the current address, if it is an instruction address, is sequential to the immediately preceding instruction address. Applicants submit that Hoyt does not teach or suggest these three signals.

The Examiner, in his rejection, indicates that the first sequence signal is taught by the hit signal in Hoyt, the second sequence signal is taught by the prediction signal in Hoyt which indicates the predicted direction of the branch (i.e. whether the branch is predicted taken or not-taken), and the third sequence signal is the branch outcome signal of Hoyt. Even if one assumes that the hit and prediction signal are the first and second sequence signals (which Applicants do not agree with for reasons provided previously), the branch outcome signal of Hoyt does not teach or suggest the third sequence signal of claims 1 and 3.

In claims 1 and 3, the third sequence signal, when negated, indicates that the current address, if it is an instruction address, is not sequential to an immediately preceding instruction address and when asserted indicates that the current address, if it is an instruction address, is sequential to the immediately preceding instruction address. Firstly, the branch outcome signal alone does not provide the same information as the claimed third sequence signal because it depends on what was predicted originally (by the prediction signal) as to whether or not the branch outcome will indicate that it is not sequential when negated and sequential when asserted. For example, the Examiner states on page 4, paragraph e of the Office Action, that "if the branch was predicted taken, for instance, when the third signal is negated (signifying correct prediction), then the current address, which is an instruction address is not sequential. On the other hand, if the third signal is asserted (signifying incorrect prediction), then the branch was really not supposed to be take, and the current address is sequential to the previous address." However, note that this only holds true when the branch was predicted taken. For example, if the branch was originally predicted not-taken, then negation of the third signal (which the Examiner has stated signifies correct prediction), then the current address (as defined by the Examiner) IS

sequential to the previous instruction. Therefore, simply the negation or assertion of the branch outcome signal of Hoyt does not indicate that the current address is not sequential or is sequential, respectively, to the immediately preceding instruction address, as claimed in claims 1 and 3. That is, if the branch outcome of Hoyt is negated (signifying correct prediction), then the current address *may or may not* be sequential to the previous address, depending on what was predicted. Similarly, if it is asserted to signify incorrect prediction, then again, the current address *may or may not* be sequential to the previous address.

Furthermore, the branch outcome signal is not provided with respect to the same current address as the first and second sequence signals, as claimed in claims 1 and 3. Although the Examiner states that the current address is not fixed but instead represents any address which is to be fetched from after the previous address, it must still be the same current address with respect to the previous address as was used for the first and second sequence signals. Note that if the Examiner assumes the previous address belongs to the branch instruction whereas the current address is the address from which to fetch an instruction immediately after the previous address, then this must be the same definition used for the third sequence signal. In paragraph 20, the Examiner provides an example in which a branch is assumed at address 0000 which has a target address of 1111. The Examiner then states that the previous address is therefore 0000 and if the branch is predicted taken, the current address is 1111. The Examiner then proceeds to state "However, if a misprediction occurs shortly thereafter, then the current address is not 1111. Instead, the current address is 0001, as this is the correct address to fetch from at this point in time. Note that in either case, both address (0001 and 1111) may be considered 'the current address' because both contain instructions which, based on the circumstance, are to be fetched immediately after fetching an instruction from the previous address." However, this is flawed logic in light of the language in claims 1 and 3. For example, for the first and sequence signals, the Examiner defines 0000 (the branch address) as the previous instruction and 1111 (the target address, i.e. the address to be fetched from) as the current instruction. In the Examiner's misprediction example, the chain of address fetches would look like **0000, 1111, 1112, ...** (sequentially down the wrong path until the branch outcome determines that it was mispredicted) **0001**. That is, at the point in time where the misprediction occurs, the Examiner redefines the current address as 0001 because "this is the correct address to fetch from *at this point in time*" (emphasis added). However, the language of claims 1 and 3 clearly state that the current address

provided on the address bus follows the previous address on the address bus without any intervening addresses. That is, if the Examiner uses 0000 as the previous address for the first and second sequence signals, then this must also be the previous address for the third sequence signal since each of the sequence signals in claims 1 and 3 are generated for *the* current address and *the* previous address. In the above example of the Examiner, if the current address is redefined at a different point in time as "0001", the Examiner can no longer state that 0000 is the "previous address" because there are many intervening address between 0000 and 0001 due to the misprediction. Therefore, while the current address may not be fixed to a particular address, it is always the one immediately following the previous address (i.e. the branch address in the Examiner's example). Therefore, the branch outcome signal is NOT a third sequence signal which indicates sequentiality of the current address (the target address of the branch in the Examiner's example) to the previous address (the address of the branch instruction). It is provided at a later point in time where the current address and the immediately preceding previous address have long been processed.

Therefore, for at least these reasons, Applicants submit that claims 1 and 3 are allowable over Hoyt. Claims 2, 4 - 9, 21 and 23 each depend, directly or indirectly, on claims 1 and 3 and therefore are allowable for at least the same reasons that claims 1 and 3 are allowable, as set forth above.

With respect to claim 21, Applicants have also clarified "in response to resolving a branch condition code" by changing it to "in response to resolving a conditional branch." The Examiner, in paragraph 24 of the current Office Action, indicates that Hoyt, in col. 8, lines 59-65, teaches that before the prediction can be provided, a type of branch must be determined, where the type field is the condition code. However, this is incorrect. Resolving a branch condition code, as known in the art, does not only refer to determining what type of branch condition is present (unconditional, conditional, return condition). However, in order to clarify claim 21, Applicants have rephrased it to "resolving a conditional branch." Simply determining what type of branch is present does not teach or suggest resolving a conditional branch. Therefore, for at least these additional reasons, Applicants submit that claims 21 is allowable over Hoyt.

Claim 24

Claim 24 also stands rejected over Hoyt. Applicants have amended claim 24 to further clarify that the first and second sequence signals are negated in a same clock cycle during which the current address is provided. The Examiner, in paragraph 27 of the current Office Action, states that these signals (referring to the hit and prediction signals of Hoyt) occur "in the same cycle so that a predicted address may be outputted for fetching purposes in the very next cycle, thereby keeping the pipeline full." However, Hoyt does not teach or suggest these signals (the hit and prediction signals) occurring in the same cycle as the predicted address (which the Examiner has indicated is the current address). Therefore, for at least these reasons, Applicants submit that claim 24 is not taught or suggested by Hoyt.

Claim 13 and its Dependent Claims

Claim 13 also stands rejected over Hoyt. Applicants have amended claim 13 to include elements of dependent claims 14 and 22 to further clarify the generation of the first and second sequence signals. In doing so, Applicants have also clarified that if the second sequence signal indicates that the address is not sequential to the immediately preceding address, the second sequence signal indicates that the address is not sequential to the immediately preceding address *in response to resolving a conditional branch.* Originally, in claim 22, Applicants claimed it was *in response to resolving a branch condition code.* However, the Examiner states in paragraph 25 of the current Office Action, that Hoyt, in col. 8, lines 59-65, teaches this because "before the second signal can be provided (the type of update to the PC), it must be determined if a branch is going to be predicted taken or not (condition code usually in the form of history bits)." However, this does not teach or suggest resolving a branch condition code, where resolving a branch condition code has a known meaning in the art. However, in order to further clarify, Applicants have claimed that it is done in response "to resolving a conditional branch." A conditional branch is *resolved* when it is *known* whether it is taken or not (i.e. at the time that the actual branch outcome is determined), and not when it is determined predicted taken or not. Therefore, the branch prediction signal of Hoyt does not indicate that the address is not sequential to the immediately preceding address in response *to resolving the conditional branch.* The conditional branch of Hoyt is not resolved until the actual branch outcome is determined.

Therefore, for at least these reasons, Applicants submit that claim 13 is not taught or suggested by Hoyt.

Claims 14 – 17, 22, and 25 each depend either directly or indirectly on claim 13 and, therefore, are allowable for at least the same reasons that claim 13 is allowable.

Claims 10 and 18 and their Dependent Claims

Claims 10 and 18 have each been amended to further clarify the timing of the first sequence signal with respect to the current address. For example, with respect to claim 10, Applicants have clarified that the "asserted or negated first sequence signal is provided with the current address." Similarly, with respect to claim 18, Applicants have clarified that "for each instruction address provided on the address bus, the first sequence signal indicating whether the instruction address is sequential to an immediately preceding instruction address is provided with the instruction address." That is, the first sequence signal is generated for a particular address *and is then provided with that address*. Applicants submit that Yoshida does not teach or suggest these elements.

The Examiner states, with respect to claim 10, that the first sequence signal is taught by Yoshida's branch prediction, where the previous address corresponds to the branch instruction, and the current address corresponds to the next address to fetch from (a sequential address if the branch is predicted not taken and a non-sequential address if the branch is predicted taken). However, since the branch prediction signal indicates from which address to be fetched from next, it must be generated prior to fetching the next address, and is therefore not provided *with the current address* (the next address to be fetched from). The branch prediction is generated prior to generating the current address and once the next address is fetched, the branch prediction for the branch instruction (previous address) is irrelevant. That is, the branch prediction signal is generated to know what the current address (the next address to be fetched from) is. At this point, though, the previously generated branch prediction signal use to generate the current address is no longer needed for the current address. Furthermore, it would unnecessarily complicate the system of Yoshida to provide this irrelevant and no longer needed signal along with the next fetch address. Thus, there is no teaching, suggestion, or even motivation to also

provide this previously generated branch prediction signal along with the current address, as claimed in claim 10. Therefore, for at least these reasons, Applicants submit that Yoshida does not teach or suggest each and every element of claim 10.

Applicants have also added dependent claim 26, depending from claim 10, to indicate that the first sequence signal is provided for use by an instruction memory. There is no teaching or suggestion in Yoshida of providing the branch prediction signal itself for use by an instruction memory. The branch prediction is an internal signal used to generate a next address, and once this address is generated using the branch prediction signal, this address (and not the branch prediction signal) is sent for fetching the instruction. That is, there is no need in Yoshida to also provide the branch prediction itself along with the current address to an instruction memory. Therefore, for these additional reasons, Applicants submit that claim 26 is also allowable over Yoshida.

Applicants have also added dependent claim 27, depending from claim 10, to indicate that when the current address is a data address, the first sequence signal is negated. There is no teaching or suggestion in Yoshida of negating the branch prediction signal during a data address. Therefore, for at least these additional reasons, Applicants submit that claim 27 is also allowable over Yoshida.

With respect to claim 18, the Examiner states that the first sequence signal is "merely any signal which dictates that a prediction is or is not to be used...for instance, a first signal exists which would cause the system to either use a predicted address for a branch (which would be non-sequential) or to use an incremented value of the program counter." However, again, this signal (which dictates whether prediction is or is not to be used) must also be generated prior to providing the address (i.e. the address for which it provides sequentiality information) because this address has to be known before it can be fetched from. Furthermore, this previously generated signal is not then provided with the address it was used to generate. Once the current address is generated and provided in Yoshida, the signal which *was* used to indicate whether prediction was or was not to be used to generate this current address is no longer needed or even relevant to the current address. Therefore, there is no teaching, suggestion, or even motivation in Yoshida to also provide this previously generated signal (which, after generating the current address, is no longer needed or relevant to the current address) along with the current address

itself. Therefore, for at least these reasons, Applicants submit that claim 18 is not taught or suggested by Yoshida.

Consequently, Yoshida fails as a 102 reference in that it does not teach each and every limitation claimed by Applicants. Therefore claims 10 and 18 are allowable over Yoshida. Claims 11, 12, 19 and 20 each depend, either directly or indirectly on claims 10 and 18 and, therefore, are allowable for at least the same reasons that claims 10 and 18 are allowable.

Conclusion

Applicants submit that the remaining claims in the Application are in condition for allowance and a Notice of Allowance is respectfully requested. If a discussion with Applicants' representative would be helpful in addressing any issues of patentability, Applicants respectfully request that the Examiner contact Applicants' attorney using the contact information provided below.

If Applicants have overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

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